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APPLICATION FOR LETTERS PATENT

FOR

LIQUID CRYSTAL DISPLAY COLUMN CAPACITANCE CHARGING WITH A CURRENT SOURCE

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LIQUID CRYSTAL DISPLAY COLUMN CAPACITANCE CHARGING WITH A CURRENT SOURCE

FIELD OF THE INVENTION

The present invention relates generally to liquid crystal display devices, and more particularly to a system and method using a current source for charging each of the liquid crystal display columns to a desired voltage.

BACKGROUND OF THE INVENTION TECHNOLOGY

Liquid crystal displays (LCDs) are commonly used in devices such as portable televisions, portable computers, control displays, and cellular phones to display information to a user. LCDs act in effect as a light valve, i.e., they allow transmission of light in one state, block the transmission of light in a second state, and some include several intermediate stages for partial transmission. When used as a high resolution information display, as in one application of the present invention, LCDs are typically arranged in a matrix configuration with independently controlled display areas called "pixels" (the smallest segment of the display). Each individual pixel is adapted to selectively transmit or block light from a backlight (transmission mode), from a reflector (reflective mode), or from a combination of the two (transflective mode).

A LCD pixel can control the transference for different wavelengths of light. For example, an LCD can have pixels that control the amount of transmission of red, green, and blue light independently. In some LCDs, voltages are applied to different portions of a pixel to control light passing through several portions of dyed glass. In other LCDs,

different colors are projected onto the area of the pixel sequentially in time. If the voltage is also changed sequentially in time, different intensities of different colors of light result. By quickly changing the wavelength of light to which the pixel is exposed an observer will see the combination of colors rather than sequential discrete colors. Several monochrome LCDs can also result in a color display. For example, a monochrome red LCD can project its image onto a screen. If a monochrome green and monochrome blue LCD are projected in alignment with the red, the combination will be a full range of colors.

The monochrome resolution of an LCD can be defined by the number of different levels of light transmission or reflection that each pixel can perform in response to a control signal. A second level is different from a first level when a user can tell the visual difference between the two. An LCD with greater monochrome resolution will look clearer to the user.

LCDs are actuated pixel-by-pixel, either one at a time or a plurality simultaneously. A voltage is applied to each pixel area by charging a capacitor formed in the pixel area. The liquid crystal responds to the charged voltage of the pixel capacitance by twisting and thereby transmitting a corresponding amount of light. In some LCDs an increase in the actuation voltage decreases transmission, while in others it increases transmission. When multiple colors are involved for each pixel, multiple voltages are applied to the pixel at different positions (different capacitance areas being charged of a pixel) or times depending upon the LCD illumination method. Each voltage controls the

transmission of a particular color. For example, one pixel can be actuated to allow only blue light to be transmitted while another allows only green. A greater number of different light levels available for each color results in a much greater number of possible color combinations.

Converting a complex digital signal that represents an image or video into voltages to be applied to charge the capacitance of each pixel of an LCD involves circuitry that can limit the monochrome resolution. The signals necessary to drive a single color of an LCD are both digital and analog. It is digital in that each pixel requires a separate selection signal, but it is analog in that an actual voltage is applied to charge the capacitance of the pixel in order to determine light transmission thereof.

Each pixel in the array of the LCD is addressed by both a column (vertical) driver and a row (horizontal) driver. The column driver turns on an analog switch that connects an analog voltage representative of the video input (control voltage necessary for the desired liquid crystal twist) to the column, and the row driver turns on a second analog switch that connects the column to the desired pixel.

The video inputs to the LCD are analog signals centered around a center reference voltage of typically from about 7.5 to 8.0 volts. A voltage called "VCOM" is not a supply voltage or signal from anywhere, but typically is a few hundred millivolts below the center reference voltage. VCOM is adjusted for best image quality, e.g., minimum flicker and/or image sticking. The center reference voltage connects to the LCD cover glass

electrode which is a transparent conductive coating on the inside face (liquid crystal side) of the cover glass. This transparent conductive coating is typically Indium Tin Oxide (ITO).

One frame of video pixels are run at voltages above the center reference voltage (positive inversion) and for the next frame the video pixels are run at voltages below the center reference voltage (negative inversion). Alternating between positive and negative inversions results in substantially a zero net DC bias at each pixel. This substantially reduces the "image sticking" phenomena.

Writing video voltage values to each pixel in, for example, an 800 x 600 (SVGA) frame takes about 2 milliseconds using 8 analog channels (DACs) in parallel operation, with each analog channel given about 25 nanoseconds to apply the appropriate video voltage value to each of its set of pixels of the SVGA frame. Unfortunately, the liquid crystal material itself takes about 3 to 4 milliseconds to settle to within one percent of its final reflectivity. That leaves very little time to flash the light source (for example: light emitting diodes – LED) for the illumination step. For example, using a three color frame image at 80 Hz, each of the color (red-green-blue) frames at 240 Hz, allows only 4.2 milliseconds per frame. Considering the requirements imposed by frame inversion, and the problem of color-breakup with color-sequential images, 80 Hz is about the slowest rate at which to present images.

Writing voltage values to columns of the LCD requires a voltage source(s) capable of rapidly charging a capacitor. The final voltage value on a column is approached exponentially in time, this time is typically from about 5 to 30 nanoseconds. The voltage source amplifier(s) used to charge the column capacitance require a large quiescent operating current in order to achieve the 5 to 30 nsec. charge time. The amount of current eventually diverted over to the LCD pixel capacitance during voltage charging thereof is infinitesimal compared to the voltage source amplifier quiescent operating current. Thus a significant amount of power is wasted in the LCD driver electronics which reduces the feasibility of using an LCD in applications requiring very low power.

What is needed is an LCD and driver that uses a minimum amount of power in its operation.

SUMMARY OF THE INVENTION

The present invention overcomes the above-identified problems as well as other shortcomings and deficiencies of existing technologies by providing a system and method for quickly and accurately writing video frame information to a matrix of pixels of a liquid crystal display (LCD) using a minimum amount of power. In accordance with exemplary embodiments of the present invention, the capacitance of each column is charged to a desired voltage by using a current source. The voltage being charged onto the column capacitance increases linearly with the current being sent thereto and is very fast (linear, not exponential). The LCD wastes no power for quiescent current (no voltage source needed). The LCD of the present invention may have its matrix of pixels

and associated support electronics, e.g., row and column selection switches and drivers, analog switches, and the like fabricated onto a semiconductor integrated circuit die, e.g., a microdisplay. The electronics controller may be fabricated on one or more semiconductor integrated circuit dice and connected to the LCD electronics.

In an exemplary embodiment, the capacitance of each column of a liquid crystal display (LCD) is charged with quantized (magnitude and time) current charges injected from a current source(s). Before charging each column capacitance, the column capacitance may be set to a known charge (precharge), e.g., a predefined voltage or no charge at all, i.e., no voltage difference between the column capacitor and the ITO layer. No charge on each of the column capacitors may be obtained by electrically connecting the columns to the ITO layer, individually or at the same time. Setting the columns to a known charge may be accomplished by connecting each of the column capacitors to a known charge or voltage source, or by connecting all of the columns together and then measuring the resulting voltage charge on any of the columns. The rows may be individually or simultaneously connected to the columns during this precharge operation so that all of the pixel capacitors are precharged to a known voltage value (either a voltage or no voltage).

A digital-to-analog converter (DAC) may be used to inject time duration controlled current pulses, using for example, but not limited to, a current mirror to charge each column capacitance to a desired voltage charge. The rate of charging is linear and fast, and has no power wastage from quiescent current in a voltage charging device as

would be needed in a voltage injection column capacitance configuration. Variations in column capacitance may be compensated for by adding capacitance so as to achieve matching column capacitance or adjusting the value of current pulses being injected and/or the time duration of the current pulses for each of the columns depending upon their capacitance.

Preferably, the capacitance of each column may be closely matched during the design and fabrication of the LCD structure. Properly designed layout and construction may render columns having substantially the same capacitance.

Another exemplary embodiment may include trimming capacitors for each of the columns so that during fabrication the capacitance of each column could be adjusted to the same average value. Fusible links may connect a plurality of capacitors for each column. These fusible links may be selectively blown to connected a desired amount of capacitance to each column so that each column has substantially the same capacitance value. The capacitors may be arranged in series-parallel combinations so that capacitance may be easily adjusted (by blowing the appropriate fuse links) for a desired total capacitance connected to each column.

Still another exemplary embodiment may use switchably controlled capacitors that may be connected to each of the columns when these columns are being charged by the current source pulses. The combination of switchably controlled capacitors required for each column may be stored in a programmable memory such as EPROM or

EEPROM, and may be determined and programmed during manufacture and testing of the LCD. When the column is selected for charging, the appropriate number of capacitors are selected through this memory.

In yet another exemplary embodiment, the voltage value on the column capacitance resulting for a given pulse amplitude and time duration period may be measured, then a correction factor may be stored in a memory and thereafter applied to modify the current pulse(s) so as to compensate for the variations of each column capacitance.

In still another exemplary embodiment, the pixels along each column may be observed and the characteristics (amplitude and pulse duration) of the current pulses adjusted for each of the columns so that substantially the same light modification characteristics are observed for each column of pixels. The characteristics so determined may then be stored in a memory for use in the normal operation of the LCD. The current pulse characteristics for each of the columns may be stored in a lookup table (LUT) such as, for example but not limited to, the gamma LUT which then may select the appropriate pulse amplitude and time duration for each of the desired gray scale shades of the LCD. Pulse repetition rate may also be used in charging the column capacitance to a desired voltage value.

A technical advantage of the present invention is in the reduction of the power required for writing frames of a liquid crystal display. Another technical advantage is

improved speed in writing a frame which reduces flicker and color-breakup artifacts. Another technical advantage is smaller and faster operating current mode digital-to-analog converters that may be imbedded into a semiconductor integrated circuit die. Still another technical advantage is obtaining a desired column voltage by controlling the pulse amplitude and/or pulse width time duration. Pulse repetition time rate may also be effectively utilized to charge the column capacitance to a desired voltage value.

Other technical advantages of the present disclosure will be readily apparent to one skilled in the art from the following figures, descriptions, and claims. Various embodiments of the invention obtain only a subset of the advantages set forth. No one advantage is critical to the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present disclosure and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, wherein:

Figure 1 is a schematic block diagram of an exemplary liquid crystal display system in accordance with exemplary embodiments of the present invention;

Figure 2 is a schematic block diagram of a portion of the liquid crystal display of Figure 1;

Figure 3 is a schematic block diagram of an exemplary embodiment of the invention;

Figure 4 is a schematic block diagram of another exemplary embodiment of the invention;

Figures 5 and 5A are schematic block diagrams of other exemplary embodiments of the invention having column voltage charge feedback sensing;

Figures 6 and 6A are schematic block diagrams of still other exemplary embodiment of the invention having automatic capacitance compensation; and

Figure 7 is a schematic block diagram of another exemplary embodiment having programmable fuse links for connecting compensation capacitors to each column.

While the present invention is susceptible to various modifications and alternative forms, specific exemplary embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

The present invention is directed to a liquid crystal display device comprising a matrix of liquid crystal pixels having light modifying properties controlled by voltage values stored in a capacitor at each of the pixel locations. A plurality of digital-to-analog converters (DACs) are coupled to the pixel matrix and are adapted to produce current pulses that are applied to columns of the pixel matrix through analog switches. The

current pulses charge each column capacitance to a desired voltage value. Row analog switches connect each column to a desired respective pixel on a selected row, thereby transferring the voltage values on the columns to the respective pixel capacitors. Voltage values on the columns may be determined by the amplitudes and/or the pulse-width times of the current pulses being injected into the columns. One or more current pulses may be used to charge each column to the desired voltage value.

Referring now to the drawings, the details of preferred embodiments of the invention are schematically illustrated. Like elements in the drawings will be represented by like numbers, and similar elements will be represented by like numbers with a different lower case letter suffix.

Figure 1 illustrates a schematic block diagram of a liquid crystal display system in accordance with exemplary embodiments of the present invention. A high-level block diagram of a system for writing voltage values to pixels of a liquid crystal display (LCD) is generally represented by the numeral 100. The voltage values being written to the pixels are representative of a frame of video data. The voltage values control the "twist" of the liquid crystal material at each pixel area so that when a light is flashed on or through the LCD, the light polarization and ultimately the intensity of the light is controlled by the "twist" of the liquid crystal material at each pixel area of the LCD.

For illustrative and exemplary purposes, the LCD 100 depicted in Figure 1 comprises a pixel matrix 102 of M rows 106 by N columns 104 for a total of M x N

individually addressable pixels 108. The combination of row control logic 110 and column control logic 112 are used to select each of the pixels 108 for writing thereto in the LCD 100, as more fully described herein. Video to pixel translation logic and a look-up table (LUT) (hereinafter translation logic) 114 perform the necessary calculations and steps to translate a video frame image 116 into discrete digital values which are sent to digital-to-analog converters (DACs) 120, 121, 122 and 123, and the pixel location addresses thereof are sent to the row and column control logic 110 and 112. It is contemplated and within the scope of the present invention that any number of DACs may be used according to exemplary embodiments of the present invention. The DACs 120, 121, 122 and 123 are current source DACs which have outputs comprising analog current values corresponding to digital input words from the translation logic 114.

Referring now to Figure 2, a schematic block diagram of a portion of the liquid crystal display system 100 of Figure 1 is illustrated. A portion of the pixel matrix 102 is represented for illustrative and exemplary purposes as pixels 108aa-108dd (4 x 4 matrix), pixel row switches 300 through 333 and pixel column switches 290 through 293. An LCD operates by charging each pixel 108aa-108dd of the LCD 100 to desired voltage values. A voltage at a pixel 108 causes liquid crystals at that pixel area to change their "twist" orientation so that light passing through the LCD 100 or being reflected is thereby affected. The translation logic 114 uses the received video frame information 116 to create appropriate voltage values which are representative of that portion of the video frame at

each one of the pixel locations. In addition, the translation logic 114 associates an x-y coordinate (row-column) location for each of these pixel voltage values.

The DACs 120-123 receive digital representations of current values from the translation logic 114 and convert these digital representations to analog current values which must then be applied to each corresponding column 104. Each column comprises a metal or other conductive material trace that is parallel with the ITO layer (transparent metal coating on the LCD front cover). The column traces are insulated from the ITO layer and the combination thereof forms the column capacitors 180, 181 and 183. Each of the pixels 108aa-108dd is formed by a "pixel mirror" which is electrically conductive and light reflective. Each of the pixel mirrors is parallel with the ITO layer and the combinations thereof form the pixel capacitors 178.

Each of the columns 0, 1 and 3 has a capacitance 180, 181 and 183, respectively, associated therewith. The capacitance 178 of each pixel may not all be the same, nor may the capacitance 180, 181 and 183 of each column be the same. However, a column capacitance, e.g., 180 is greater than a pixel capacitance, e.g., 178. In the exemplary embodiments, an analog current value charges a respective column capacitance to a desired voltage value (after the column capacitance has been precharged to a certain value, e.g., all columns present to the same charge voltage value or discharged to zero voltage value). The current pulse output of the DAC is connected to the column and thereby charges the column capacitance to a desired analog voltage, each pixel in a selected row is connected to a corresponding column (the row pixels may be connected to the respective columns either

before or after the respective columns are charged). Therefore, the voltage on the pixel will be substantially the same as the voltage on the corresponding column.

For example, a column(s) is charged to a certain voltage while a pixel row is selected so that the intersection(s) thereof is the desired pixel to be charged. For example, columns 0-3 are charged from the DACs 120-123, respectively, when the column switches 290-293 are closed. Pixels 108aa-108ad are charged from the columns 0-3, respectively, when the row switches 300-303 are closed (row 0). A plurality of DACs may be used to simultaneously charge a like number of columns, then a like number of switches in a row may be used to charge a like number of pixels from the respective charged columns. The column control logic 112 and row control logic 110 control operation of the column switches 290-293 and row switches 300-333, respectively, for the group of pixels 108aa-108dd. Other pixel groups 108 are controlled in a similar fashion.

Referring now to Figure 3, a schematic block diagram of an exemplary embodiment of the invention is illustrated. The current DACs 120-123 are adapted to receive digital current amplitude information from a gray scale current pulse look up table 354. The gray scale current pulse look up table 354 receives pixel grayscale information from the video frame to LCD pixel address and gray scale conversion logic 352 which is adapted to convert video information 116 into corresponding pixel information (grayscale and pixel address information). Pixel address information is sent to an LCD pixel address controller 356 which is adapted to control the row control logic 110 and column control logic 112. The gray scale current pulse look up table 354 determines the

necessary current pulse amplitude and pulse-width time duration for charging the column capacitance to a desired voltage for transfer to the respective pixel. The voltage to which the column capacitance is charged is a function of the integral of the current pulse amplitude over a period of time divided by the capacitance of the column, and any initial voltage charge on the column capacitance. The energy stored in the column after being charged to the desired voltage is one-half the capacitance of the column times the voltage squared. For example, power consumption (energy times time) of an 800 x 600 pixel RGB LCD operating at 100 Hz and having an average column capacitance of one picofarad (1E-12) would be for a worse case black frame (V = 13 volts):

$$0.5 \times 1E\text{-}12 \times 13 \times 13 \times 800 \times 600 \times 3 \times 100 = 12 \text{ milliwatts}$$

Therefore, each column capacitance may be charged to a desired voltage value by applying the correct current amplitude and width time pulse to the column. Generally since the pixel is already connected to its respective column, the column voltage is thereby transferred to the pixel capacitance.

Referring now to Figure 4, a schematic block diagram of another exemplary embodiment of the invention is illustrated. The gray scale current pulse look up table 354 may control the current pulse amplitude and/or pulse width time of the current DAC 120. For example, a binary digital value is applied at the input 406 of the DAC 120 which controls the amplitude value of the current from the output of the DAC 120 which is connected to switch 408. The binary digital value may be of any bit size, e.g., 10 bits is 1024 different current amplitude values. A switch 408 may be used to control the pulse

width time of the output current from the DAC 120. The pulse width time may be selected from a frequency at a clock input 412. The clock input 412 may be from an output of a phase-locked-loop (PLL) 410. The PLL 410 may be used to multiply the frequency of the column clock and also to synchronize the pulse width time control 402 to the column clock. For example, a column clock (Col_Ck) frequency may be multiplied by ten so that there are ten different pulse width selections available using a four bit binary or BCD signal at input 404, or eight different pulse width selections using a three bit binary signal at input 404. For example, using an 10 bit amplitude word and a four bit pulse-width time word results in being able to programmably charge over 10,000 different voltage values on the column capacitance.

Referring now to Figure 5, a schematic block diagram of another exemplary embodiment of the invention having column voltage charge feedback sensing is illustrated. Video information 116 is received by the video frame to LCD pixel address and gray scale conversion logic 352 and is converted into pixel information for display on the LCD matrix 102 (Figure 1). The pixel information from the LCD pixel address and gray scale conversion logic 352 is applied to a gray scale voltage look-up table 528 which converts the pixel gray scale information into an equivalent gray scale digital voltage value required at the pixel so as to obtain the desired gray scale shade from the liquid crystal. This gray scale digital voltage value may be any number of bits in size, e.g., an 8 bit binary word.

A gray scale current pulse look-up table 504 converts the gray scale digital voltage value is into a digital current pulse value for controlling the amplitude value of a current pulse from the DAC 120. The gray scale current pulse look-up table 504 may also control the time duration (width) of the current pulse using the pulse width time control 402 and current output switch 408. The functional purpose of the switch 408 may be integral with the DAC 120, e.g., an internal disable or shut down circuit in the DAC 120. The current pulse width may be selected according to the granularity of a clock input 412, e.g., from a phase-locked-loop (PLL) 410 which may be synchronized to a column clock (Col_Ck) input 414. In the example illustrated in Figure 5, a selection from 1 to 10 of the column clock is available when a 4 bit pulse-width time selection value is at the input 404 of the pulse width time control 402.

Column capacitance values may vary from one column to another, therefore current pulses having the same value will not charge to the same voltage columns having different capacitance values. This may be compensated for using this exemplary embodiment by measuring a resulting voltage on a column after a current pulse has voltage charged that column. A compensation coefficient may be determined for each column which may be factored with a general current pulse value e.g., amplitude and pulse-width (for all columns) to produce substantially the same voltage on each column even though each column may have a different capacitance. Switch 518 may be closed to connect the voltage charged column to an analog-to-digital converter (ADC) 516. The ADC 516 measures the column voltage by converting the analog voltage to a digital voltage value that may be input to

digital comparator 526 or may be input directly to the gray scale current pulse look-up table 504 which also comprises a column compensation memory.

A comparison is made of the digital voltage value from the ADC 516 (representing the actual voltage on the column) and the desired gray scale voltage value for that column. If the comparison results in a difference between the desired and actual voltages on the column, a correction factor may be stored in the column compensation memory so that any variation from one column capacitance to another is thereby compensated for and the same gray scale current pulse value for a certain pixel voltage from the gray scale voltage look-up table 528 may be used regardless of any variations in the column capacitance. Column capacitance variation compensation may be performed upon start-up of the LCD system 100, during a test and calibrate mode, or performed during normal operation of the LCD system 100.

Referring now to Figure 5A, a schematic block diagram of another exemplary embodiment of the invention having column voltage charge feedback sensing is illustrated. Video information 116 is received by the video frame to LCD pixel address and gray scale conversion logic 352 and is converted into pixel information for display on the LCD matrix 102 (Figure 1). The pixel information from the LCD pixel address and gray scale conversion logic 352 is applied to a gray scale voltage look-up table 528 which converts the pixel gray scale information into an equivalent gray scale digital voltage value required at the pixel so as to obtain the desired gray scale shade from the liquid crystal.

This gray scale digital voltage value may be any number of bits in size, e.g., an 8 bit binary word.

A gray scale current pulse look-up table 504 converts the gray scale digital voltage value is into a digital current pulse value for controlling the amplitude value of a current pulse from the DAC 120. The gray scale current pulse look-up table 504 may also control the time duration (width) of the current pulse using the pulse width time control 402 and current output switch 408. The functional purpose of the switch 408 may be integral with the DAC 120, e.g., an internal disable or shut down circuit in the DAC 120. The current pulse width may be selected according to the granularity of a clock input 412, e.g., from a phase-locked-loop (PLL) 410 which may be synchronized to a column clock (Col_Ck) input 414. In the example illustrated in Figure 5, a selection from 1 to 10 of the column clock is available when a 4 bit pulse-width time selection value is at the input 404 of the pulse width time control 402.

Column capacitance values may vary from one column to another, therefore current pulses having the same value will not charge to the same voltage columns having different capacitance values. This may be compensated for using this exemplary embodiment by measuring a resulting voltage on a column after a current pulse has voltage charged that column. A compensation coefficient may be determined for each column which may be factored with a general current pulse value e.g., amplitude and pulse-width (for all columns) to produce substantially the same voltage on each column even though each column may have a different capacitance.

Switch 518 may be closed to connect the voltage charged column to an input of an analog voltage comparator 566. Another input of the comparator 566 is connected to a DAC 556. The DAC 556 generates an analog voltage from digital information from the gray scale voltage look-up table 528. The comparator 566 determines whether the voltage from switch 518 (representing the actual voltage on the column) is less than, equal to, or greater than the voltage from the DAC 556, the desired gray scale voltage value for that column. It is contemplated and within the scope of the present invention that the DAC 556 and comparator 566 functions may be combined into one mixed signal (analog and digital) comparator circuit having a single analog input, a digital reference value input, and a comparison output.

The results of the comparison from the comparator 566 is output to the gray scale current pulse look-up table 504. If the comparison results in a difference between the desired and actual voltages on the column, a correction factor may be stored in the column compensation memory 504 so that any variation from one column capacitance to another is thereby compensated for and the same gray scale current pulse value for a certain pixel voltage from the gray scale voltage look-up table 528 may be used regardless of any variations in the column capacitance. Column capacitance variation compensation may be performed upon start-up of the LCD system 100, during a test and calibrate mode, or performed during normal operation of the LCD system 100.

Referring now to Figure 6, a schematic block diagram of another exemplary embodiment of the invention having automatic capacitance compensation is illustrated.

Video information 116 is received by the video frame to LCD pixel address and gray scale conversion logic 352 and is converted into pixel information for display on the LCD matrix 102 (Figure 1). The pixel information from the LCD pixel address and gray scale conversion logic 352 is applied to a gray scale voltage look-up table 528 which converts the pixel gray scale information into an equivalent gray scale digital voltage value required at the pixel so as to obtain the desired gray scale shade from the liquid crystal. This gray scale digital voltage value may be any number of bits in size, e.g., an 8 bit binary word.

A gray scale current pulse look-up table 504 converts the gray scale digital voltage value is into a digital current pulse value for controlling the amplitude value of a current pulse from the DAC 120. The gray scale current pulse look-up table 504 may also control the time duration (width) of the current pulse using the pulse width time control 402 and current output switch 408. The functional purpose of the switch 408 may be integral with the DAC 120, e.g., an internal disable or shut down circuit in the DAC 120. The current pulse width may be selected according to the granularity of a clock input 412, e.g., from a phase-locked-loop (PLL) 410 which may be synchronized to a column clock (Col_Ck) input 414. In the example illustrated in Figure 6, a selection from 1 to 10 of the column clock is available when a 4 bit pulse-width time selection value is at the input 404 of the pulse width time control 402.

Column capacitance values may vary from one column to another, therefore current pulses having the same value will not charge to the same voltage columns having different capacitance values. This may be compensated for using this exemplary embodiment by

adding capacitance to a column to achieve an average value of capacitance for each column. Columns having a larger capacitance would require little or no added capacitance and columns having a smaller capacitance would require a greater amount of capacitance added thereto. Capacitors 620 are controllably connected to a column through switches 622 which are controlled by a column capacitance compensation circuit 624. The capacitors 620 may be arranged in a binary value order, e.g., capacitor 620a is 8C, capacitor 620b is 4C, capacitor 620c is 2C and capacitor 620d is C, where C is the capacitor value.

The required amount of capacitance to be added to each column may be determined by measuring a resulting voltage on a column after a current pulse has voltage charged that column. Switch 518 may be closed to connect the voltage charged column to an analog-to-digital converter (ADC) 516. The ADC 516 measures the column voltage by converting the analog voltage to a digital voltage value that may be input to comparator 526. A comparison is made of the digital voltage value from the ADC 516 (representing the actual voltage on the column) and the desired gray scale voltage value for that column. If the comparison results in a difference between the desired and actual voltages on the column, the column capacitance compensation 624 can increase or decrease the amount of capacitance of the column by switching an appropriate value of the capacitors 620. The required selection of the capacitors 620 may then be stored in a column compensation memory 626 so that any variation from one column capacitance to another is thereby compensated for and the same gray scale current pulse value for a certain pixel voltage from the gray scale voltage look-up table 528 may be used regardless of any variations in the

column capacitance. For example, column selection information may be obtained from the column switch control logic 112. Column capacitance variation compensation may be performed upon start-up of the LCD system 100, during a test and calibrate mode, or performed during normal operation of the LCD system 100.

Referring now to Figure 6A, a schematic block diagram of another exemplary embodiment of the invention having automatic capacitance compensation is illustrated. Video information 116 is received by the video frame to LCD pixel address and gray scale conversion logic 352 and is converted into pixel information for display on the LCD matrix 102 (Figure 1). The pixel information from the LCD pixel address and gray scale conversion logic 352 is applied to a gray scale voltage look-up table 528 which converts the pixel gray scale information into an equivalent gray scale digital voltage value required at the pixel so as to obtain the desired gray scale shade from the liquid crystal. This gray scale digital voltage value may be any number of bits in size, e.g., an 8 bit binary word.

A gray scale current pulse look-up table 504 converts the gray scale digital voltage value is into a digital current pulse value for controlling the amplitude value of a current pulse from the DAC 120. The gray scale current pulse look-up table 504 may also control the time duration (width) of the current pulse using the pulse width time control 402 and current output switch 408. The functional purpose of the switch 408 may be integral with the DAC 120, e.g., an internal disable or shut down circuit in the DAC 120. The current pulse width may be selected according to the granularity of a clock input 412, e.g., from a phase-locked-loop (PLL) 410 which may be synchronized to a column clock (Col_Ck)

input 414. In the example illustrated in Figure 6, a selection from 1 to 10 of the column clock is available when a 4 bit pulse-width time selection value is at the input 404 of the pulse width time control 402.

Column capacitance values may vary from one column to another, therefore current pulses having the same value will not charge to the same voltage columns having different capacitance values. This may be compensated for using this exemplary embodiment by adding capacitance to a column to achieve an average value of capacitance for each column. Columns having a larger capacitance would require little or no added capacitance and columns having a smaller capacitance would require a greater amount of capacitance added thereto. Capacitors 620 are controllably connected to a column through switches 622 which are controlled by a column capacitance compensation circuit 624. The capacitors 620 may be arranged in a binary value order, e.g., capacitor 620a is 8C, capacitor 620b is 4C, capacitor 620c is 2C and capacitor 620d is C, where C is the capacitor value.

The required amount of capacitance to be added to each column may be determined by measuring a resulting voltage on a column after a current pulse has voltage charged that column. Switch 518 may be closed to connect the voltage charged column to an input of an analog voltage comparator 566. Another input of the comparator 566 is connected to a DAC 556. The DAC 556 generates an analog voltage from digital information from the gray scale voltage look-up table 528. The comparator 566 determines whether the voltage from switch 518 (representing the actual voltage on the column) is less than, equal to, or greater than the voltage from the DAC 556, the desired gray scale voltage value for that

column. It is contemplated and within the scope of the present invention that the DAC 556 and comparator 566 functions may be combined into one mixed signal (analog and digital) comparator circuit having a single analog input, a digital reference value input, and a comparison output.

This determination is output from the comparator 566 to the column capacitance compensation circuit 624. If the desired voltage (from the gray scale voltage look-up table 528) and the actual voltage on the column (from switch 518 are not equal then the column capacitance compensation 624 can increase or decrease the amount of capacitance of the column by switching an appropriate value of the capacitors 620. The required selection of the capacitors 620 may then be stored in a column compensation memory 626 so that any variation from one column capacitance to another is thereby compensated for and the same gray scale current pulse value for a certain pixel voltage from the gray scale voltage look-up table 528 may be used regardless of any variations in the column capacitance. For example, column selection information may be obtained from the column switch control logic 112. Column capacitance variation compensation may be performed upon start-up of the LCD system 100, during a test and calibrate mode, or performed during normal operation of the LCD system 100.

The required selection of the capacitors 620 may determined during manufacture and/or final testing of the LCD. The desired selection of the capacitors 620 for each column 104 may be stored in an electrically programmable read only memory (EPROM)

or electrically erasable and programmable read only memory (EEPROM) which may comprise the column capacitance memory 626.

Referring to Figure 7, depicted is a schematic block diagram of another exemplary embodiment having programmable fuse links for connecting compensation capacitors to each column. A column 104 may be connected to a plurality of capacitors 720 that are connected in a series-parallel combination. Fuse links 722 are further connected to the series-parallel combination of capacitors 720 and are adapted to be selectively blown during manufacturing and/or final testing of the LCD. Certain ones of the fuse links 722 are blown (open) so as to put in a parallel connected capacitor 720 or remove a series connected capacitor(s) 720 for compensating the column 104 capacitance. Each of the columns 104 may have a series-parallel connected compensation capacitor array so that during manufacture and/or final testing each of the columns 104 may be adjusted to have substantially the same capacitance. Three separate series connected capacitor strings are illustrated (720a, 720b and 720c) but one of ordinary skill in the art will readily understand, having the benefit of this disclosure, that any number and connection combination of capacitors 720 and fuse links 722 may be utilized for compensating the capacitance of each column 104.

It is contemplated and within the scope of the embodiments of the present invention that the LCD and LCD system may be partially or entirely fabricated on a semiconductor integrated circuit.

The invention, therefore, is well adapted to carry out the objects and attain the ends and advantages mentioned, as well as others inherent therein. While the invention has been depicted, described, and is defined by reference to exemplary embodiments of the invention, such references do not imply a limitation on the invention, and no such limitation is to be inferred. The invention is capable of considerable modification, alternation, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent arts and having the benefit of this disclosure. The depicted and described embodiments of the invention are exemplary only, and are not exhaustive of the scope of the invention. Consequently, the invention is intended to be limited only by the spirit and scope of the appended claims, giving full cognizance to equivalents in all respects.